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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:)	
Ming-Dou KER et al.)	Examiner: Alonzo Chambliss
Serial No.: 09/818,449)	Art Unit: 2827
Filed: March 27, 2001)	Docket No.: 4280-D2
For: Low-capacitance bonding pad for semiconductor device)	

AMENDMENT AND RESPONSE TO OFFICE ACTION

Assistant Commissioner of Patents and Trademarks
Washington, DC 20231

Sir:

The Office Action mailed on January 17, 2002 has been carefully considered. In response thereto, please enter the following amendments and consider the following remarks.

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AMENDMENTS

In The Drawings

See attached Drawing Amendment sheet.

In The Specification

Please amend the specification as follows.

In the paragraph beginning at page 12, line 8

BR/ -- This issue can also be solved by the invention. By means of the stacked metal layer 208, the bonding pad opening 270 can be placed right above the device region. As a result, more substrate surface can be favorably available. --

In the paragraph beginning at page 12, line 15

BR/ -- Referring to Fig. 23, a device 32, such as a field effect transistor, is formed on a substrate 30. Metal layers 51, 52, 53, 54, 55 and 56 are formed in a dielectric layer 60 over the device 32, in which the dielectric layer 60 serves as an isolation and a frame to stack the metal layers 51, 52, 53, 54, 55, 56. The dielectric layer 60 may further include several sub-layers to hold and isolate the metal layers. A bonding pad includes the metal layers 55 and 56 and is covered by a passivation layer 80. The passivation layer 80 includes a bonding pad opening 82 which exposes a portion of the metal layer 56. The metal layers 51 and 52 near the substrate 30 serve as, for example, signal lines electrically connected to the substrate 30 by means of via plug 70, and the metal layers 53 and 54 are designed to be planar layers and serve as, for example, power lines. The passivation layer 80 is formed on the dielectric layer 60, and the bonding pad

opening 82 is formed in the passivation layer 80 to expose the metal layer 56. A bonding wire 84 is attached to the metal layer 56 within the bonding pad opening 84. Each pair of the metal layers 51, 52, 53, 54, 55 and 56 is isolated by the dielectric layer 60. The metal layers 55, 56 are coupled by a via plug 75 and the metal layers 51, 52 are coupled by a via plug 71. The metal layers 52, 53 and 54 serving as signal lines and power lines are also coupled by via plugs (not shown) as well as the metal layers 54 and 55. However, these via plugs should not be formed under the bonding pad opening 82. Thus, the metal layers 53, 54 can be used as buffer layers, and the bonding stress on the active devices can be reduced through these buffer layers. --

In The Claims

Please amend the claims as follows.

26. (Once amended) A low-capacitance bonding pad for a semiconductor device, comprising:

a substrate;

a stack of metal layers alternating with dielectric layers on the substrate, wherein the metal layers are coupled with one another by a plurality of via plugs in the dielectric layers, the via plugs being placed in alternating manner with respect to one another through the stack;

an uppermost metal layer positioned on the stack and electrically connected to the stack, wherein an area of each metal layer in the stack is smaller than that of the uppermost metal layer; and

a passivation layer having a bonding pad opening positioned on the uppermost metal layer for externally electric connection.

Sub 7
C2 28. (Once amended) A low-capacitance bonding pad for a semiconductor device,
comprising:

Py a substrate;

a stack of metal layers alternating with dielectric layers on the substrate, wherein the metal layers are coupled with one another by a plurality of via plugs through the dielectric layers and are placed in a concentric circle arrangement;

an uppermost metal layer positioned on the stack and electrically connected to the stack;
and

a passivation layer having a bonding pad opening on the uppermost metal layer for externally electric connection.

B5 30. (Once amended) A low-capacitance bonding pad for a semiconductor device,
comprising:

a substrate having a well;

Sub 7
C3 a doped region formed in the well as a diffusion region; and

a bonding pad on the substrate, the bonding pad comprising a stack of metal layers alternated with dielectric layers and an uppermost metal layer, the metal layers and the uppermost metal layer being electrically connected to one another by a plurality of via plugs through the dielectric layers, wherein the bonding pad being aligned with the doped region.

Sub 4
C4 36. (Once amended) A semiconductor device, comprising:

B6 a substrate having a well;

a doped region formed in the well as a diffusion region;

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a bonding pad on the substrate, the bonding pad comprising a stack of metal layers alternated with dielectric layers and an uppermost metal layer, the metal layers and the uppermost metal layer being electrically connected to one another by a plurality of via plugs through the dielectric layers, wherein the bonding pad is aligned with the doped region, and wherein the metal layers in the stack are in a concentric circle arrangement; and
a device under the bonding pad.

Sub 37
39. (Once amended) A semiconductor device, comprising:

133
a substrate having a well;

a doped region formed in the well as a diffusion region;

a bonding pad on the substrate, the bonding pad comprising a stack of metal layers alternated with dielectric layers and an uppermost metal layer, the metal layers and the uppermost metal layer being electrically connected to one another by means of a plurality of via plugs, wherein the bonding pad is aligned with the doped region; and wherein an area of each metal layer in the stack is smaller than that of the uppermost metal layer; and
a device under the bonding pad.

REMARKS

Present Status of the Application

The Office Action dated January 17, 2002 rejected all the pending claims 26-41 of the above-identified application. Claim 26 was rejected under 35 USC 102(b) as being anticipated by Oku et al. (US Patent No. 5,394,013, hereafter "Oku"). Claims 27-41 were rejected under 35 USC 103(a) as being unpatentable over the above Oku in view of Yuan (US Patent No. 5,838,043). Claims 26 and 28 were further objected to because of minor language informality. The Office Action further objected to the drawings as failing to comply with 37 CFR 1.84(p)(5) because they include reference signs not mentioned in the description.

The Applicants have carefully considered the remarks set forth by the Office Action to the present application. In this response and amendment paper, claim 26 has been amended to patently define over the prior art. Claims 28, 30, 36, and 39 have been further amended to include limitations that clarify the claimed invention. Furthermore, the specification and the drawings have been amended to overcome the drawing objections. No claims have been deleted and no new matter has been introduced by way of the amendments made in this response. In view of the foregoing amendments and the following remarks, the Applicants respectfully request the reconsideration and allowance for the claims.

Discussion of the Office Action Objections

Discussion of the drawing objection

The Office Action objected to the drawings as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference signs not mentioned in the description: 34, 70, and

550.

The Applicants apologize for the typographical error of Fig. 7. The reference sign "550" of Fig. 7 has replaced with the reference sign 750 in accordance with the description of page 9, lines 4-14. In accordance with the illustration of Fig. 23, the specification has been amended to include the description related to the reference sign 70, as set forth in the above amendments.

With respect to the reference signs 34, the Applicants respectfully submit that the specification at page 13 line 12 explicitly describes the reference sign 34 as an n-well located in the substrate 30.

In view of the above, the Applicants thus respectfully request the withdrawal of the objections.

Discussion of the Office Action Rejections

Discussion of the claim rejection under 35 USC 102

The Office Action rejected claim 26 under 35 USC 102(b) as being allegedly anticipated by Oku. Claim 26 has been amended, and the Applicants accordingly respectfully traverse the rejection.

As described in FIG. 6A and col. 9, lines 1-15, Oku discloses a bonding pad structure in which metal layers 29b, 71b, and 45 are alternated with dielectric layers 19, 21, 73 in a stack structure. Aluminum metals formed in through holes 44, 46 electrically connect the metal layers 29b to the metal layer 71b and the metal layer 71b to the metal layer 45, respectively. Oku teaches the through holes 44, 46 be formed on the corresponded underlying metal layer to achieve electrical connection between the metal layers, and no further guidelines are depicted with respect to specific arrangement of the through holes (see for example col. 9, lines 1-15).

At most it can be ascertained, the drawings illustrate the through holes be formed in an overlapping fashion so that a metallic central film 11a is electrically connected to the active region of the gate electrode 41 and source/drain 35, 37 while being sideways offset therefrom.

In light of the above, Oku thus clearly fails to disclose and suggest the claimed invention in which the bonding pad comprises **a plurality of via plugs that are placed in an alternating manner** through the dielectric layers to electrically connect the different metal layers in the stack. As taught in the specification page 7, lines 20-24, such an arrangement favorably prevents peel-off effect.

For at least the above reasons, the Applicants thus respectfully submit that amended claim 26, reciting the above limitation, patentably define over the prior art reference.

Discussion of the claim rejection under 35 USC 103

The Office Action further rejected claims 27-41 under 35 USC 103(a) as being unpatentable over Oku in view of Yuan. The Applicants respectfully traverse the rejection.

As discussed above, Oku lacks limitations that are included in the claimed invention. Oku is further silent about the specific shape of the metal layers, and clearly fails to disclose and suggest the concentric circle arrangement of the metal layers as disclosed in the claimed invention. As taught in page 11, lines 20-24, this disposition enables a reduction of the overlapping area of the metal layers over the substrate, thereby favorably reducing the parasitic capacitance of the bonding pad.

With respect to claims 27, 28, 33, 36, and 40, none of the cited references thus adequately teach and suggest the claimed invention in which the metal layers are placed in a concentric

circle arrangement. As discussed above, this particular arrangement allows the reduction of the overlapping area of the metal layers over the substrate, thereby favorably reducing the parasitic capacitance. As a result, the Applicants respectfully submit the rejection set forth in the Office Action is improper.

Furthermore, Yuan illustrates a bonding pad 22 as being formed over the circuit devices (see FIG. 2 through FIG. 4 and col. 3, lines 10-24) to provide electrical connection. Unlike Oku, Yuan does not disclose any specific structures of the bonding pad. However Yuan may suggest a bonding pad that is *above* the circuit reduces the parasitic capacitance, but Yuan still fails to disclose the bonding pad being **aligned with the doped region as a diffusion region** in the substrate, as taught in the claimed invention. The specification at page 12, lines 5-7 further discloses a disadvantage of having the bonding pad as taught by Yuan, possibly causing a damage of the active device region when bonding wire is bonded onto the bonding pad. Yuan's structure teaches away from the above guidelines implemented in Oku's bonding pad where a the stack of metal layers electrically connected by means of the through holes are clearly directed to **offset sideways** the central film 11a from the active device region of the gate 41.

In consideration of the above, the asserted combination of Oku with Yuan is thus insufficient to properly teach the claim limitations. With respect to claims 30, 36, and 39, the Applicants thus respectfully submit that none of the cited references, independently taken or combined with one another, adequately teach and suggest the claimed invention in which the bonding pad is aligned with the doped region.

By virtue of their dependency on patentable independent claims 26, 28, 30, 36, and 39 as

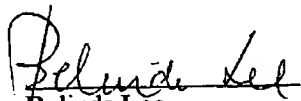
discussed above, claims 29, 31, 32, 34, 35, 37, 38, and 41 should be also patentable over the prior art.

CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 26-41 of the present invention are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

Date: March 27, 2002


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